Macnica SLVS-EC RX IP for Intel

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Macnica Advanced Technology
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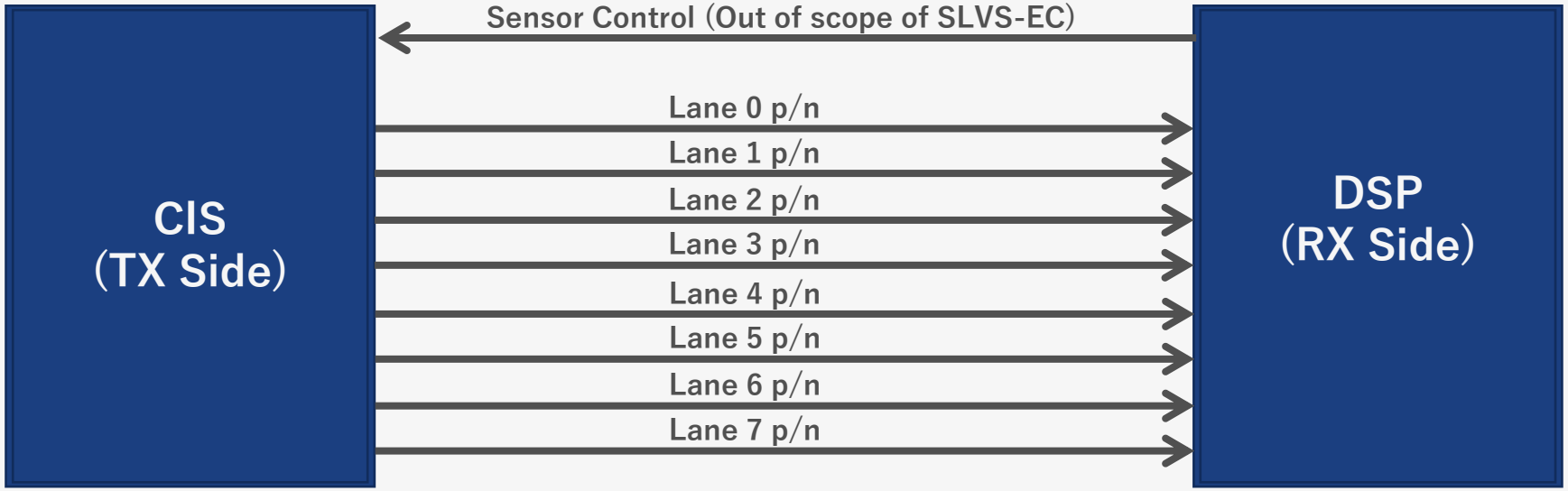
Co.Tomorrowing

MACNICA

SLVS-EC Overview



Function	Description
Lane Num	1, 2, 4, 6, 8 (Max 8 Lane)
Baud Rate	1.152 to 1.25 Gbps (Baud Grade 1)
	2.304 to 2.5 Gbps (Baud Grade 2)
	4.608 to 5.0 Gbps (Baud Grade 3)
Encode	ANSI 8B10B
Clock Type	Embedded clock (CDR)

Features of SLVS-EC RX IP

- Supported Features

Features		SLVS-EC Full Spec	Macnica IP supports
Lane Num		1, 2, 4, 6, 8	✓
Baud Rate	Grade1 (1.152 to 1.25 Gbps)	✓	✓
	Grade2 (2.304 to 2.5 Gbps)	✓	✓
	Grade3 (4.608 to 5.0 Gbps)	✓	✓
Bit par Pixel		8, 10, 12, 14, 16	✓
CRC		✓	✓
ECC(Option)		Option 1, 2	✓
Standby		✓	✓
Dynamic Mode Change		✓	✓
Embedded Data		✓	✓
Symbol Control		✓	✓

FPGAs supported by Macnica IP for Intel

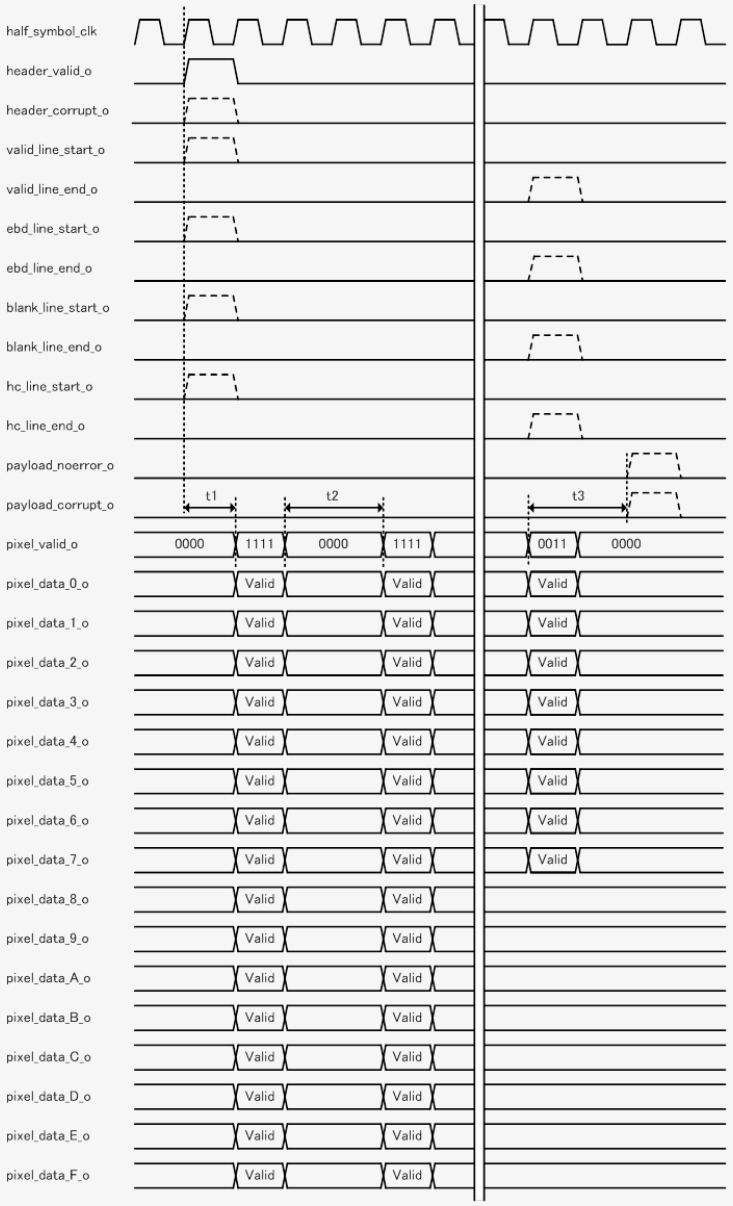
- Supported FPGA families
  - Cyclone V
  - Cyclone 10
  - Arria 10
  - Stratix 10

FPGA Vendor	Family	Baud Rate		
		Grade1	Grade2	Grade3
Intel	Cyclone V	✓	✓	-
	Cyclone10	✓	✓	✓
	Arria10	✓	✓	✓
	Stratix10	✓	✓	✓

✓ feasible
- not feasible
* feasible with ECC option disabled

Note : The table above is just a guideline to choose device family depending on Baud Rate. Please note that the actual feasibility differs depending on the device's speed grade and resource congestion etc.. We strongly recommend to check your design with an evaluation license before purchasing, especially in the case you need to use Baud Grade3.

Overview of Pixel Data I/F



- 16 Pixels are output in parallel with 4-bit valid signals (each bit corresponds to 4 pixels), regardless of the number of the SLVS-EC lanes used.
- Signals indicating which type of line starts/ends (valid pixel, blanking, embedded, a line after header error)

Demo configuration

- RAW bit stream received via SLVS-EC is output to CoaXPress v2.0

Baud Grade 3
Raw12, 5328x4672 pix @74.5fps
Reed-Solomon Error Correction Enabled

Deliverables

- IP Package
  - Encrypted RTL
    - Evaluation Ver. Restrictions
      With 30 min time-limited
      Free license for 3 months evaluation
  - Simulation Design
    - Supported Tool: Mentor Graphics
    - Testbench & simulation RTL
  - IP User's manual
- Reference Design
  - Example connection between IP and Transceiver
  - User's Guide